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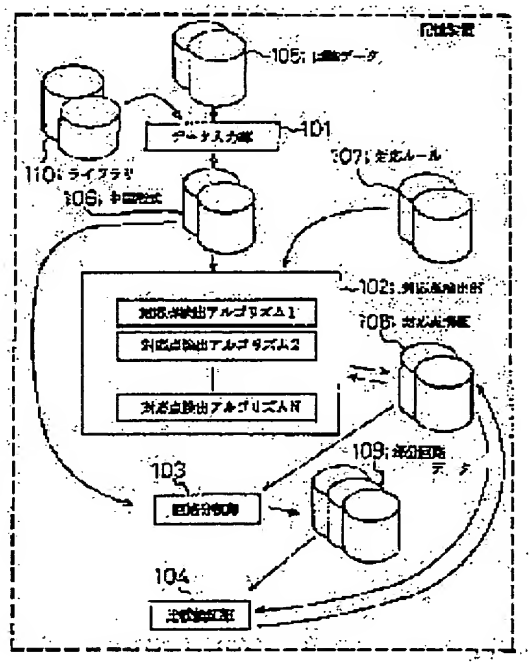
(54) DEVICE AND METHOD FOR LOGIC CIRCUIT VERIFICATION

(57)Abstract:

PROBLEM TO BE SOLVED: To automatically extract a partial circuit from a large-scale circuit while considering circuit constitution and to reduce the operation man-hour of a user, by referring to partial circuit data and corresponding point information and comparing and verifying divided circuit data.

SOLUTION: By a data input part 101, circuit data 105 are read. A part using a library in the circuit data 105 is replaced by the read logic information of a library 110. Also, the logic information of the circuit data 105 is extracted and an intermediate form 106 is outputted. A corresponding point detection part 102 reads an intermediate form 106, uses a corresponding point detection algorithm, detects a corresponding point to be used at the time of comparison of a circuit and output it to corresponding point information 108. A circuit division part 103 reads the intermediate form 106, divides a circuit while referring to the corresponding point information 108 and outputs the partial circuit data 109. When the partial circuit data 109 are prepared, a comparison and verification part 104 compares corresponding data and writes the result to the corresponding point information 108.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to logical circuit verification equipment and the logical circuit verification approach.

[0002]

[Description of the Prior Art] In order to have performed identification nature verification of two circuits conventionally, paying attention to the register, partial division of the circuit was carried out first.

[0003] Moreover, using middle signal name information, partial division of the circuit was carried out further, the partial circuit compared from register signal name information or middle signaling information was matched, and equivalence verification was performed for every matched partial circuit.

[0004] As for register signal name information or middle signaling information, a user needs to be specified.

[0005] As this kind of a conventional technique, the publication of reference (the "logic verification system CONDOR" besides Mukoyama, the design-automation study group 63-3, the 17 - 22nd page, Information Processing Society of Japan) is referred to, for example. The system configuration of this conventional technique is shown in drawing 10 .

[0006]

[Problem(s) to be Solved by the Invention] As shown in drawing 10 by the approach stated to the above-mentioned reference, in the logic collating section, circuit division is performed by the register and the middle signal, and although comparison collating is carried out about the divided partial circuit, there is not the Ruhr which matches which [of a dividing network / which and which] are compared.

[0007] In order not to take circuitry into consideration, there is no other way but to specify [of the dividing network to compare] in the conventional method.

[0008] Therefore, this invention is made in view of the above-mentioned situation, and the purpose is in offering the logical circuit verification equipment and the logical circuit verification approach which make it possible not to specify matching of the partial circuit to

compare with an one-point one-point help, to carry out automatic extracting based on the Ruhr, or to extract automatically in consideration of circuitry, and reduced a user's activity man day by this.

[0009]

[Means for Solving the Problem] In order to attain said purpose, the logical circuit verification equipment of this invention The means which reads circuit information from circuit data or a library about a logical circuit, and carries out the conversion output of this logical circuit at the intermediate form independent of technology, The information on the corresponding points for opting for matching of with which to compare which about the part which divides said logical circuit into a partial circuit, and the divided partial circuit A corresponding-points detection means to extract using 1 or two or more corresponding-points detection algorithms, and to output as corresponding-points information, A circuit division means to output the partial circuit data which come to divide said logical circuit into a partial circuit based on said corresponding-points information and the circuit information on said intermediate form, With reference to said partial circuit data and said corresponding-points information, comparison verification of the divided circuit data is carried out, and it is characterized by having a comparison verification means to output the result.

[0010] In this invention, it is characterized by acquiring the information on the corresponding points which coincidence of an identifier and/or an identifier read about a signal, a logical name, etc., and are compared with reference to the Ruhr, such as a regulation, in the case of the extract of said corresponding-points detection means of corresponding points.

[0011] Moreover, in this invention, said comparison verification means is characterized by outputting a comparison verification result to said corresponding-points information.

[0012] Moreover, in case the logical circuit verification approach of this invention performs identification nature verification of two or more logical circuits Circuit information is read from circuit data or a library about this logical circuit. Change into the intermediate form which does not depend for this logical circuit on technology, and 1 or two or more corresponding-points detection algorithms are used from this intermediate form. The corresponding points of the external output terminal of the circuit to compare and/or the node inside a circuit are extracted, and it divides into a partial circuit about the circuit of corresponding-points information and said intermediate form, and is characterized by

matching the partial circuit compared from said corresponding-points information and said divided partial circuit for a deed and identification nature verification.

[0013] Moreover, by traversing the logic node of the circuit which should be compared based on said corresponding-points information, in consideration of circuitry, partial division of the circuit is carried out and it is characterized by performing identification nature verification in the logical circuit verification approach of this invention.

[0014]

[Embodiment of the Invention] The gestalt of operation of this invention is explained below with reference to a drawing.

[0015] Drawing 1 is drawing showing the configuration of the gestalt of operation of this invention. If drawing 1 is referred to, the gestalt of operation of the 1st of this invention is equipped with the data input section 101, the corresponding-points detecting element 102, the circuit division section 103, and the comparison verification section 104, and is constituted.

[0016] Two or more algorithms for detecting corresponding points are stored in the corresponding-points detecting element 102. Here, the external output terminal of the circuit in comparison with "corresponding points" or the output terminal in a circuit is said. Exchange, and the use / intact selection of these algorithms (the corresponding-points detection algorithm 1 - N) is enabled.

[0017] The corresponding-points detecting element 102 is equipped with the correspondence Ruhr 107 used with a corresponding-points algorithm, and the corresponding-points information 108 which stores corresponding points.

[0018] The circuit data 105 consist of netlists, such as hardware description languages, such as VHDL (IEEE1076) and Verilog-HDL (IEEE1364), and EDIF.

[0019] A library 110 is data the logic information on the macro used in the circuit data 105 was described to be with the above-mentioned hardware description language or the netlist.

[0020] Moreover, an intermediate form 106 is data for storing circuit information.

[0021] The partial circuit data 109 are a file as a result of the circuit division section's 103 dividing an intermediate form 106 into a partial circuit.

[0022] An intermediate form 106, the corresponding-points information 108, and the partial circuit data 109 are temporarily stored and used for storage.

[0023] Drawing 2 is a flow chart for explaining the processing flow of the gestalt of operation

of this invention. Actuation of the gestalt of operation of this invention is explained with reference to the flow chart of drawing 1 and drawing 2 .

[0024] The circuit data 105 are read by the data input section 101 (step 201). When the macro in a library is being used in the circuit data 105 in that case, the part for which a library 110 is also read into coincidence and is using the library in the circuit data 105 is replaced by the logic information on the read library 110. Moreover, the logic information on the circuit data 105 is extracted, and it outputs to an intermediate form 106.

[0025] Next, the corresponding-points detecting element 102 detects the corresponding points which read an intermediate form 106, use a corresponding-points detection algorithm, and are used at the time of the comparison of a circuit, and outputs them to the corresponding-points information 108 (step 202). In order that a corresponding-points detection algorithm may find corresponding points, when using the Ruhr in that case, it reads from the correspondence Ruhr 107. Moreover, it is also possible to register two or more corresponding-points detection algorithms, and it can specify whether it is used if needed.

[0026] Next, the circuit division section 103 reads an intermediate form 106, it performs circuit division, referring to the corresponding-points information 108, and outputs the partial circuit data 109 (step 203).

[0027] If the partial circuit data 109 are created, the comparison verification section 4 will compare corresponding data, and will write the result in the corresponding-points information 108 (step 204). In the comparison verification section 4, a test pattern is generated for the comparison of a circuit using the verification technique and ATPG (Automatic Test Pattern Generator) which used BDD (Binary Decision Diagram), and the verification technique which performs simulation is used for it.

[0028] Verification in the comparison verification section 104 is repeated until the verification for all of circuits finishes.

[0029] Next, with reference to the flow chart of drawing 3 , the corresponding-points detection algorithm using the correspondence Ruhr is explained.

[0030] First, the Ruhr which read the correspondence Ruhr and was specified is interpreted (step 401). Next, the partial circuit which corresponds from circuit data according to the Ruhr is extracted (step 402). Next, corresponding-points information is outputted (step 403). If it judges whether all the Ruhr was applied (step 404) and there is the Ruhr which has not been

applied about it, return and when all are applied, processing will be ended to step 402.

[0031] Next, with reference to drawing 5 , the correspondence Ruhr 107 shown in drawing 1 is explained.

[0032] The correspondence Ruhr consists of limitation 603 of the Ruhr 601, the corresponding location 602, a signal, and logic.

[0033] The Ruhr 601 consists of the identifier coincidence Ruhr 604 and the identifier reading substitute Ruhr 605. Among these, the identifier coincidence Ruhr 604 is the Ruhr which makes corresponding points the point whose character string of an identifier corresponds, and the identifier reading substitute Ruhr 605 is the Ruhr for searching the corresponding points of the circuit in comparison with the basis of a fixed regulation, even when the character string of an identifier is not in agreement.

[0034] The corresponding location 602 specifies whether the part which applies the Ruhr is a signal name, or (signal name 606 of drawing 5) it is an instance name (unique identifier logic was named) (instance name 607 of drawing 5).

[0035] The limitation 603 of a signal and logic is for limiting the case where the Ruhr is applied, and consists of the signal classification 608, the logic classification 609, a specific signal 610, and a specific instance 611.

[0036] The signal classification 608 specifies the external terminal of a circuit, and an internal terminal. The Ruhr is applied the specified signal classification or in addition to it.

[0037] The logic classification 609 specifies logic (AND, OR, register, etc.). The Ruhr is applied in addition to the specified logic or the specified logic.

[0038] The specific signal 610 specifies a signal name. The Ruhr is applied the specified signal name or in addition to it.

[0039] The specific instance 611 specifies an instance name. The Ruhr is applied the specified instance name or in addition to it.

[0040] Assignment of the corresponding location 602 is enabled for every Ruhr, and the limitation 603 of a signal and logic can specify it for every corresponding location. Moreover, the limitation 603 of a corresponding location 602 and a corresponding signal, and logic can also change the contents dynamically.

[0041] Next, with reference to drawing 9 , the corresponding-points information 108 shown in drawing 1 is explained to a detail.

[0042] The corresponding-points information 108 consists of the group 1006 of an output terminal 1005 and an input terminal, corresponding points 1007, and a comparison verification result 1008.

[0043] An output terminal 1005 holds the signal used as the output terminal at the time of carrying out circuit division. The group 1006 of the input terminal corresponding to an output terminal 1005 holds the signal used as the input signal at the time of carrying out circuit division. Corresponding points 1007 hold the output terminal used as the corresponding-points information name of another circuit in comparison with an output terminal 1005, and the candidate for a comparison.

[0044] The comparison verification result 1008 holds whether the result was in agreement, after carrying out comparison verification of the two circuits.

[0045] One example of this invention is explained below that the gestalt of operation of above-mentioned this invention should be further explained to a detail.

[0046] First, the given circuit data are read and an intermediate form 106 is generated in the data input section 101.

[0047] An intermediate form 106 consists of a hierarchy 801 and circuit information 802, as shown in drawing 7 .

[0048] A hierarchy 801 points out the hierarchy relation of a circuit, and the circuit information 802 corresponding to each hierarchy.

[0049] Each hierarchy's logic information is stored in the circuit information 802. As shown in drawing 7 , the connection relation of logic is expressed with an input terminal 803, logic 804, and an output terminal 805 in the circuit information 802.

[0050] The identifier of an input terminal and an output terminal is acquired from the signal name 806. The instance name attached to logic is acquired from the instance name 807.

[0051] In order to know signal classification, for example, an external input pin, the signal classification 808 has pointed out the signal name for every classification.

[0052] In order to know logic classification, for example, a register, the logic classification 809 has pointed out the instance name for every classification.

[0053] The signal name 806, the instance name 807, the signal classification 808, and the logic classification 809 are effective in order to search a signal and logic efficiently from the limitation 603 of the correspondence location 602 specified, a signal, and logic in the

correspondence Ruhr (refer to drawing 5).

[0054] The correspondence Ruhr 107 is read with the intermediate form 106 generated from the data input section 101, corresponding points are detected by the corresponding-points detecting element 102, and the result is outputted to the corresponding-points information 108.

[0055] Drawing 6 shows an example (example) of the correspondence Ruhr 107 in this example. In drawing 6 , the identifier shows the conditions that all matches consider that the identifier coincidence Ruhr 701 is corresponding points about an external input terminal and an external output terminal.

[0056] First, the corresponding-points detecting element 102 follows the signal name 806 from the external output terminal of the signal classification 808 (refer to drawing 7) in an intermediate form 106, follows an output terminal 805 from the signal name 806 further, and outputs the table index of an output terminal 805 to the output terminal 1005 (refer to drawing 9) of the corresponding-points information 108.

[0057] With reference to drawing 6 , the identifier reading substitute Ruhr 702 shows that logic matches AA00, AA01, --, AA19 with XX00, XX01, --, XX19 about the instance of a register.

[0058] In this case, the corresponding-points detecting element 102 follows logic 804 from the instance name 807 from the logic classification 809 (refer to drawing 7) of an intermediate form 106, and an instance name, further, follows an output terminal 805 from logic 804, and outputs the table index of an output terminal 805 to the output terminal 1005 (refer to drawing 9) of the corresponding-points information 108.

[0059] With reference to drawing 9 , the corresponding-points information file name of the circuit to compare and the table index of an output terminal 1005 are written in corresponding points 1007.

[0060] If all the correspondence Ruhr is applied, retrieval will be continued in the input direction until it reaches the signal memorized by the external input terminal or another output terminal 1005 from the signal memorized by the output terminal 1005.

[0061] The input signal of the point which reached is memorized to the group 1006 of an input terminal.

[0062] In the circuit division section 103, the corresponding-points information 109 is read, a

circuit is divided using the information on the group 1006 (refer to drawing 9) of an output terminal 1005 (refer to drawing 9) and an input terminal, and it outputs to the partial circuit data 109.

[0063] In the comparison verification section 104, partial circuit day 109 TA is read, a test pattern is generated using the verification technique which used BDD (Binary Decision Diagram) for the comparison of a circuit, and ATPG (Automatic Test Pattern Generator), and it verifies by performing simulation.

[0064] The verification result in the comparison verification section 104 is memorized to the comparison verification result 1008 (refer to drawing 9) of corresponding-points information.

[0065] Next, the gestalt of operation of the 2nd of this invention is explained. Drawing 4 is a flow chart for explaining the processing flow of the gestalt of operation of this invention. With reference to drawing 4 , the corresponding-points detection algorithm in consideration of circuitry in the gestalt of operation of the 2nd of this invention is explained.

[0066] With reference to drawing 4 , the external input terminal (it is called "PI") of the circuit data to compare and the output terminal (it is called "temporary PI") whose comparison verification result corresponds by the output terminal stored in corresponding-points information are read first (step 501).

[0067] Next, a logic node (the output terminal of logic, such as AND and OR, is called "logic node") is searched in the output direction of a circuit from PI and temporary PI (step 502).

[0068] With reference to the input terminal of a logic node, when the number of input terminals is one, a logic node is further searched in the output direction (steps 503 and 504).

[0069] Even if an input terminal is plurality, when the signal value of other input terminals is being fixed to "0" and "1", the retrieval to the output direction is continued similarly (steps 503 and 504).

[0070] And when a register is reached, retrieval is stopped there (step 503).

[0071] next, from the output terminal ("-- it is called temporary PO") of the logic node which reached, it follows in the input direction of a circuit and searches in PI or temporary PI (step 505).

[0072] and temporary -- the output terminal 1005 (refer to drawing 9) of the corresponding-points information 108 and the combination of temporary PI are memorized for PO in the group 1006 (refer to drawing 9) of the input terminal of the corresponding-points information

108 (step 505).

[0073] By judgment processing of step 506, processing of step 502 to the step 505 is repeated to all PI and temporary PI.

[0074] The above-mentioned processing is repeated about all the circuits to compare. That is, step 501' of drawing 4 - 506' show the processing flow about another circuit which should be compared.

[0075] next, temporary in the circuits to compare -- the combination of PI and temporary PI to PO compares by finding a match (steps 507-509).

[0076] In the case of an inequality, inequality information is outputted (steps 510 and 511).

[0077] next, the comparison was finished -- temporary -- PO is memorized as temporary PI (step 512).

[0078] judgment processing of step 513 -- all -- temporary -- processing of step 507 to the step 512 is repeated about PO.

[0079] all -- temporary -- when the verification about PO finishes, temporary PI investigates whether it newly generated. When temporary PI is found, return processing is continued first (step 514).

[0080] The example of this invention is explained below with reference to a drawing that the gestalt of operation of the 2nd of above-mentioned this invention should be further explained to a detail.

[0081] An example of the circuit data for explaining this example to drawing 8 is shown.

[0082] First, the corresponding-points detecting element 102 reads the corresponding-points information 108.

[0083] Here, in the circuit data shown in drawing 8 , temporarily, Terminal E is memorized by the output terminal 1005 (refer to drawing 9), and if it assumes that it is that whose comparison verification result corresponds, it can be considered that this terminal E is temporary PI.

[0084] Next, with reference to drawing 7 , the signal name 806 is followed from the signal classification 808 of an intermediate form, an input terminal 803 is followed further, and the external input terminals A, B, C, and D (refer to drawing 8) are set to PI.

[0085] Next, one of the PI "A" is taken out, a logic node is searched in the output direction, and "G1" is reached (refer to drawing 8).

[0086] Since the number of input terminals is one, "G1" continues the retrieval to the output direction, and it reaches a logic node "G2" (refer to drawing 8).

[0087] As shown in drawing 8 , since two input terminals are equipped with "G2", it stops retrieval here. temporary in the output terminal "H" of "G2" -- it is referred to as PO.

[0088] Next, it searches in the input direction from "G2", and "E" is reached. Since "E" is temporary PI, it stops retrieval here.

[0089] The output terminal 1005 (refer to drawing 9), "A", and "E" of the corresponding-points information 108 are memorized for "H" in the group 1006 (refer to drawing 9) of an input terminal.

[0090] Since "B" and "C" are already registered into the group of the input terminal 1006 of the corresponding-points information 108, nothing carries out them, but they search for "D" which is remaining PI, and memorize the output terminal 1005 (refer to drawing 9) of the corresponding-points information 108, "D", and "E" for "I" in the group 1006 (refer to drawing 9) of an input terminal.

[0091] Processing with the same said of the circuit to compare is performed, and out of corresponding-points information, the group of an input chooses a match and performs circuit division in the circuit division section 103.

[0092] In the example of this example, the partial circuit to "H" and "I" is generated. Similarly, it divides into a partial circuit also about the circuit used as the candidate for a comparison.

[0093] And comparison verification is performed in the comparison verification section 104.

[0094] Temporarily, the partial circuit "H", "I", and for [corresponding to this] a comparison is found, and suppose that the verification result was in agreement. In this case, "H" and "I" are set to temporary PI.

[0095] Next, "H" and "I" which newly turned into temporary PI are processed.

[0096] First, it follows in the output direction from "H", and reaches to "G3." Although the number of input terminals is one, since "G3" is an external terminal, a stop and "F" are memorized to the output terminal 1005 (refer to drawing 9) of the corresponding-points information 108, and the output terminal "F" of "G3" memorizes "H" for retrieval in the group 1006 (refer to drawing 9) of an input terminal here.

[0097] Next, processing with the same said of "I" is performed, "G" is memorized to the

output terminal 1005 (refer to drawing 9) of the corresponding-points information 108, and I is memorized in the group 1006 (refer to drawing 9) of an input terminal.

[0098] Processing with the same said of the circuit to compare is performed, and out of corresponding-points information, the group of an input chooses a match, performs circuit division in the circuit division section 103, and performs comparison verification in the comparison verification section 104 further.

[0099] Moreover, if it assumes that a result is inharmonious by "I" among "H" and "I", it will judge that it was unsuitable to have made "I" into corresponding points, and will go to find corresponding points again.

[0100] It searches in the output direction about corresponding points "I", and the output "G" of "G6" is reached. The output terminal 1005 (refer to drawing 9) of the corresponding-points information 108, and "E" and "D" are memorized for "G" in the group 1006 (refer to drawing 9) of an input terminal. And comparison verification is performed and a result is stored in the comparison verification result 1007 (refer to drawing 9).

[0101]

[Effect of the Invention] As explained above, even when signal names, such as a register, differ according to this invention, by having presupposed that it is possible to pinpoint the partial circuit compared automatically in consideration of circuitry, the activity man day that a user specifies the signal name to compare can be excluded, and the increase in efficiency of a logic verification process is attained.

CLAIMS

[Claim(s)]

[Claim 1] The means which reads circuit information from circuit data or a library about a logical circuit, and carries out the conversion output of this logical circuit at the intermediate form independent of technology, The information on the corresponding points for opting for matching of with which to compare which about the part which divides said logical circuit into a partial circuit, and the divided partial circuit A corresponding-points detection means to extract using 1 or two or more corresponding-points detection algorithms, and to output as corresponding-points information, A circuit division means to output the partial circuit data which come to divide said logical circuit into a partial circuit based on said corresponding-points information and the circuit information on said intermediate form, Logical circuit verification equipment which carries out comparison verification of the divided circuit data with reference to said partial circuit data and said corresponding-points information, and is characterized by having a comparison verification means to output the result.

[Claim 2] Logical circuit verification equipment according to claim 1 characterized by acquiring the information on the corresponding points which coincidence of an identifier and/or an identifier read about a signal, a logical name, etc., and are compared with reference to the Ruhr, such as a regulation, in the case of the extract of said corresponding-points detection means of corresponding points.

[Claim 3] Logical circuit verification equipment according to claim 1 with which said comparison verification means is characterized by outputting a comparison verification result to said corresponding-points information.

[Claim 4] The logical circuit verification equipment according to claim 1 characterized by to include the corresponding points which consist of an identifier of the storing means of the information on the group of the input terminal corresponding to the information on an output terminal that said corresponding-points information serves as a terminal in the case of circuit division, and this output terminal, and the corresponding-points information on other circuits compared with said output terminal, and an output terminal used as the candidate for a comparison, and the information on the coincidence/the inequality which it is as a result of comparison verification of the circuit for [in said comparison verification means] a

comparison.

[Claim 5] Logical circuit verification equipment according to claim 1 with which said circuit division means is characterized by reading said corresponding-points information and dividing the circuit of said intermediate form into a partial circuit from the information on the group of the output terminal of this corresponding-points information, and an input terminal.

[Claim 6] Logical circuit verification equipment according to claim 1 which traverses the logic node of the circuit compared based on said corresponding-points information, and is characterized by dividing a circuit into a partial circuit and performing comparison verification in consideration of the circuitry of the circuit which should be compared.

[Claim 7] About the external input terminal (it is called "PI") of the circuit to compare, and the output terminal (it is called "temporary PI") whose comparison verification result corresponds by the output terminal contained in said corresponding-points information When it searches for a logic node from said external input terminal to an output side and two or more input edges or registers are reached It searches until it reaches said PI or temporary PI to an input side from the output terminal (it is called "PO") of the logic node which reached. The above-mentioned processing is performed [circuit / to compare] about all PI and temporary PI. temporary about said circuit to compare -- the logical circuit verification equipment according to claim 1 characterized by for the combination of PI and temporary PI to PO comparing by finding a match, dividing a circuit into a partial circuit in consideration of circuitry, and performing comparison verification.

[Claim 8] In case identification nature verification of two or more logical circuits is performed, circuit information is read from circuit data or a library about this logical circuit. Change into the intermediate form which does not depend for this logical circuit on technology, and 1 or two or more corresponding-points detection algorithms are used from this intermediate form. The corresponding points of the external output terminal of the circuit to compare and/or the node inside a circuit are extracted. The logical circuit verification approach characterized by matching the partial circuit which divides into a partial circuit about the circuit of corresponding-points information and said intermediate form, and is compared from said corresponding-points information and said divided partial circuit for a deed and identification nature verification.

[Claim 9] The logical circuit verification approach according to claim 8 which carries out

partial division of the circuit and is characterized by performing identification nature verification in consideration of circuitry by traversing the logic node of the circuit which should be compared based on said corresponding-points information.

[Claim 10] Logical circuit verification equipment characterized by matching the partial circuit which uses one or more algorithms, divides into a partial circuit and is compared with it for a deed and identification nature verification when performing identification nature verification of two or more circuits.

[Claim 11] Logical circuit verification equipment according to claim 10 characterized by carrying out partial division of the circuit in consideration of circuitry, and performing identification nature verification in said logical circuit verification equipment.

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１０４　比較検証部
１０５　回路データ
１０６　中間形式
１０７　対応ルール
１０８　対応点情報
１０９　部分回路データ
１１０　ライブラリ
６０１　ルール
６０２　対応する場所
６０３　信号，論理の限定
６０４　名前一致ルール
６０５　名前読み替えルール
６０６　信号名
６０７　インスタンス名
６０８　信号種別
６０９　論理種別
６１０　特定信号

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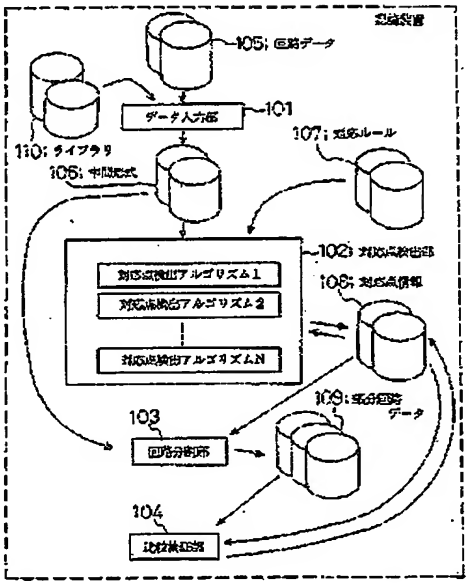
＊６１１　特定インスタンス
７０１　名前一致ルールの一例
７０２　名前読み替えルールの一例
８０１　階層情報
８０２　回路情報
８０３　入力端子
８０４　論理
８０５　出力端子
８０６　信号名
８０７　インスタンス名
８０８　信号種別
８０９　論理種別
１００５　出力端子
１００６　入力端子の組
１００７　対応点
１００８　比較検証結果

＊

【図１】



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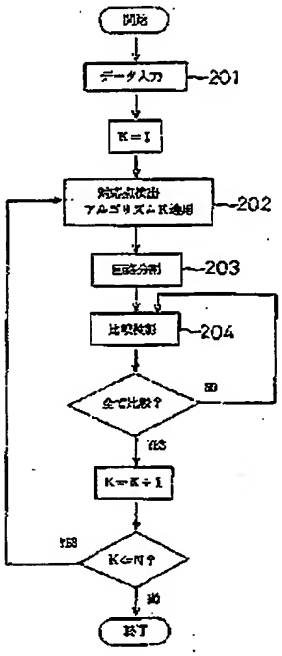

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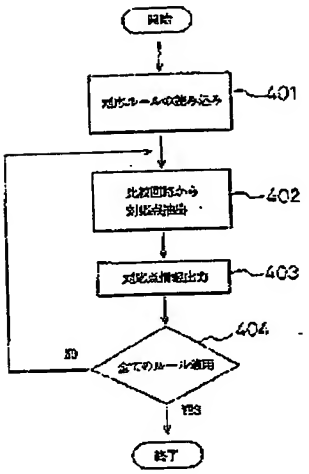
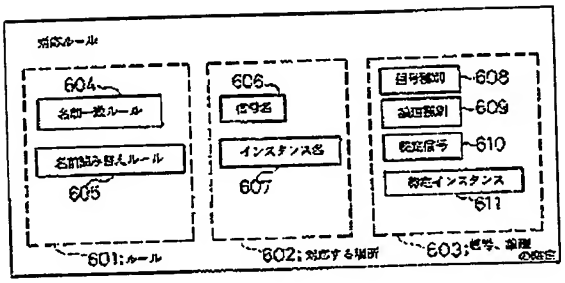
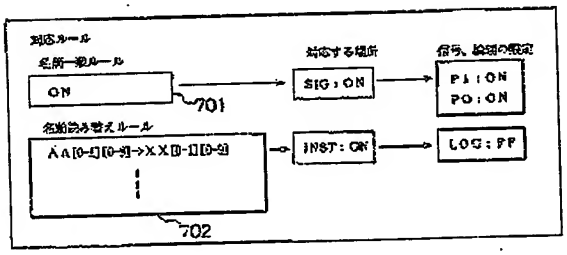

開始
対応ルールの読み込み
401
比較回路から
対応情報抽出
402
対応表情報出力
403
404
全てのルール適用
NO
YES
終了

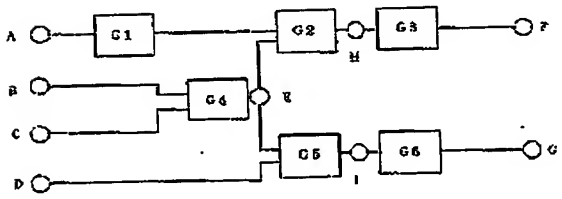
【図5】


対応ルール
604
名前一致ルール
名前読み替えルール
605
606
信号名
インスタンス名
607
608
609
610
611
601:ルール
602:対応する場所
603:信号、論理の設定

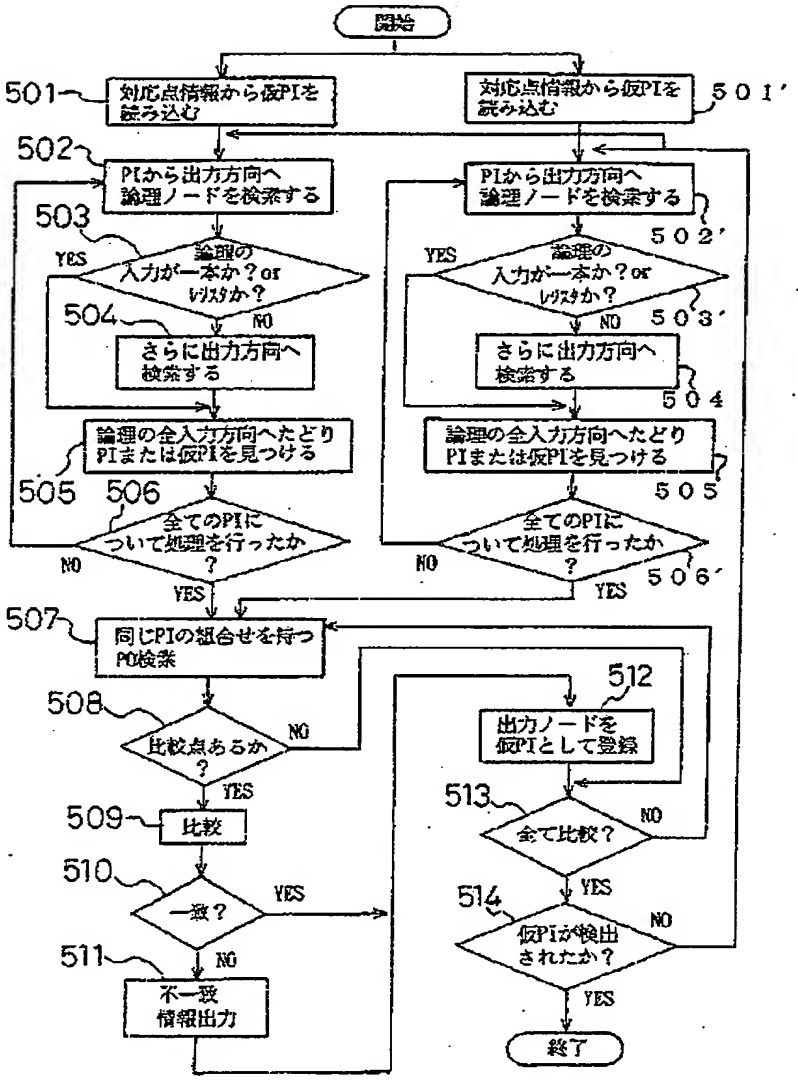
【図6】


対応ルール
名前一致ルール
ON
701
対応する場所
SIG:ON
信号、論理の設定
P1:ON
P0:ON
名前読み替えルール
AA[0-9][0-9]→XX[0-9][0-9]
INST:ON
LOG:FF
702

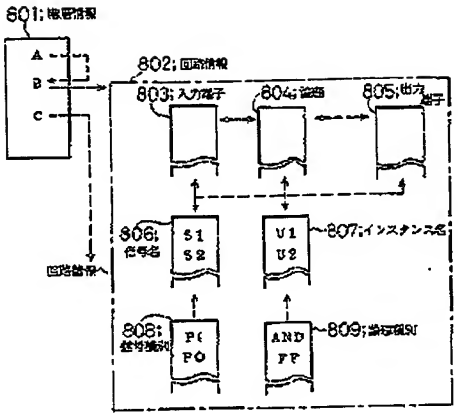
【図8】


A
B
C
D
G1
G2
G3
G4
G5
G6
H
I

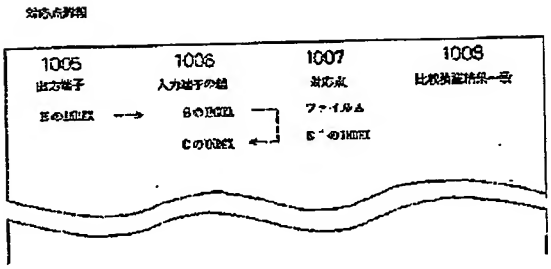
【図4】


開始
501
対応点情報から仮PIを読み込む
501'
対応点情報から仮PIを読み込む
502
PIから出力方向へ論理ノードを検索する
502'
PIから出力方向へ論理ノードを検索する
503
論理の入力が一本か？or レジスタか？
503'
論理の入力が一本か？or レジスタか？
YES
NO
504
さらに出力方向へ検索する
504
さらに出力方向へ検索する
505
論理の全入力方向へたどりPIまたは仮PIを見つける
505
論理の全入力方向へたどりPIまたは仮PIを見つける
506
全てのPIについて処理を行ったか？
506'
全てのPIについて処理を行ったか？
NO
YES
507
同じPIの組合せを持つPO検索
508
比較点あるか？
NO
YES
509
比較
510
一致？
YES
NO
511
不一致情報出力
512
出力ノードを仮PIとして登録
513
全て比較？
NO
YES
514
仮PIが検出されたか？
NO
YES
終了

【図7】


801;
A
B
C
802;
803;
804;
805;
806;
信号名
S1
S2
807;インスタンス名
V1
U2
回路結線へ
808;
P(
PO
AND
FF
809;

【図9】


1005
出力端子
1006
入力端子の組
1007
対応表
1008

【図１０】